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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,420	FOLEY, MICHAEL P.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 6, 2004 was filed after the mailing date of the application on October 30, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-11 and 13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-11 and 13 are directed to a method for reordering data between a first predefined order and a second predefined order, but do not set forth an application of the method to produce a tangible result (i.e. using the result (data arranged in the second predefined order) to display the data). The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result (*State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02). The tangible requirement requires that the claim must set forth a practical application of the 101 judicial exception to produce a real-world result (*Benson*, 409 U.S. at 71-

72, 175 USPQ at 676-77). See MPEP 2106 II A. Since there is no tangible result recited in these claims, these claims are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-7, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US005960213A) in view of Childers (US005793996A).

7. With regard to Claim 1, Wilson discloses a method for reordering data between a first predefined order and a second predefined order using a secondary processor (GLINT Delta) to perform the reordering, thereby offloading the reordering of the data from a primary processor

(host processor), the secondary processor reordering the data between the first predefined order and the second predefined order, the method comprising the steps of enabling the secondary processor to access the data that are arranged in the first predefined order (*Delta Unit in the GLINT Delta implements data conversion for graphics primitives in one unit, GLINT Delta accepts texture parameters, the operations in the Delta Unit remove a considerable amount of work from the host processor*, Col. 2, lines 43-64; *GLINT Delta can accept and convert gib-endian data*, Col. 4, lines 20-25; Col. 20, lines 4-10). According to the disclosure of this application, reordering the data using an operation that was not provided for that purpose involves using texture operations to perform the reordering (page 11, lines 20-22). Wilson discloses that the GLINT Delta performs operations such as texture operations (Col. 2, lines 47-62), and since the GLINT Delta is performing the reordering, Wilson discloses reordering the data using an operation that was not provided for that purpose.

However, Wilson does not teach determining subdivisions of the data that are arranged in the first predefined order, wherein each subdivision is based on a predefined size of each datum of the data; determining original positions of coordinates defining each subdivision within the data that are arranged in the first predefined order; and causing the secondary processor to perform the operation, which transforms the coordinates of each subdivision to new positions and repositions the data of each subdivision to have the same locations relative to the new positions as the data had relative to the original positions, thereby reordering the data from the first predefined order to the second predefined order. However, Childers discloses that each pixel contains 2 bytes (16 bits) of data (Col. 4, lines 61-64; Figures 4A, 4B). The data are subdivided into half-words (16 bits) in order to ensure that pixels are presented in a uniform

format regardless of the endian characteristic of the bus from which they were received or of the software or apparatus that generated the pixels (Col. 8, lines 32-42), so that the pixels themselves do not become "scrambled" as a result of their bytes being swapped (Col. 4, line 48-Col. 5, line 16). Therefore, Childers discloses determining subdivisions of the data that are arranged in the first predefined order (little-endian, Col. 20, lines 40-45; Col. 8, lines 36-42), wherein each subdivision is based on a predefined size (2 bytes) of each datum (pixel) of the data (Col. 4, lines 61-64; Col. 8, lines 32-42); determining original positions of coordinates defining each subdivision within the data that are arranged in the first predefined order; and causing the processor to perform the operation, which transforms the coordinates of each subdivision to new positions and repositions the data of each subdivision to have the same locations relative to the new positions as the data had relative to the original positions, thereby reordering the data from the first predefined order to the second predefined order (Col. 17, line 54-Col. 18, line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson to include determining subdivisions of the data that are arranged in the first predefined order, wherein each subdivision is based on a predefined size of each datum of the data; determining original positions of coordinates defining each subdivision within the data that are arranged in the first predefined order; and causing the secondary processor to perform the operation, which transforms the coordinates of each subdivision to new positions and repositions the data of each subdivision to have the same locations relative to the new positions as the data had relative to the original positions, thereby reordering the data from the first predefined order to the second predefined order as suggested by Childers because Childers suggests the advantage of guaranteeing that pixels are placed into their proper location

and also that the bytes within the pixel are in the proper order (Col. 4, line 48-Col. 5, line 16; Col. 8, lines 32-42; Col. 17, line 54-Col. 18, line 2).

8. With regard to Claim 2, Wilson discloses that the secondary processor comprises a graphics processor (Col. 2, lines 43-48, 63-64; Col. 4, lines 20-25; Col. 20, lines 4-10).

9. With regard to Claim 3, Wilson does not specifically teach what the first and second predefined orders are. According to the disclosure of this application, pixilated endian order means that the data is subdivided as a function of pixel size (page 4, lines 10-12). Therefore, Childers discloses that one of the following conditions exists: (c) the first predefined order comprises a pixilated little endian order, and the second predefined order comprises a big endian order; and (d) the first predefined order comprises a pixilated big endian order, and the second predefined order comprises a little endian order (Col. 8, lines 36-42; *it need not be the case that the system bus 301 is big-endian and the expansion bus 329 is little-endian; the invention can easily be adapted for use in a system in which the reverse is true*, Col. 20, lines 40-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson so that one of the following conditions exists: (c) the first predefined order comprises a pixilated little endian order, and the second predefined order comprises a big endian order; and (d) the first predefined order comprises a pixilated big endian order, and the second predefined order comprises a little endian order as suggested by Childers because Childers suggests the advantage of interconnecting two buses of otherwise incompatible types (Col. 5, lines 31-33) and the advantage of guaranteeing that pixels are placed into their

proper location and also that the bytes within the pixel are in the proper order (Col. 4, line 48-Col. 5, line 16; Col. 8, lines 32-42; Col. 17, line 54-Col. 18, line 2).

10. With regard to Claim 4, Wilson discloses that the data comprise image data (Col. 2, lines 43-48, 63-64; Col. 4, lines 20-25; Col. 20, lines 4-10).

11. With regard to Claim 5, Wilson discloses that the operation comprises one of a draw operation and a multi-textured draw operation (Col. 2, lines 43-48, 63-64; Col. 4, lines 20-25; Col. 19, line 65-Col. 20, line 10).

12. With regard to Claim 6, Wilson does not teach that the step of enabling the secondary processor to access the data comprises the steps of predefining a secondary storage space that is accessible to the secondary processor; causing the primary processor to store the data in the first predefined order in a primary storage space that is accessible to both the primary processor and the secondary processor; and causing the secondary processor to copy the data in the first predefined order from the primary storage space to the secondary storage space. However, Childers discloses that the step of enabling the secondary processor (511, Figure 5) to access the data comprises the steps of predefining a secondary storage space (523) that is accessible to the secondary processor; causing the primary processor (531) to store the data in the first predefined order in a primary storage space (517) that is accessible to both the primary processor and the secondary processor; and causing the secondary processor to copy the data in the first predefined order from the primary storage space to the secondary storage space (*video input device 531 is*

connected to an expansion bus 529 and supplies pixel data that needs to be written to the frame buffer 517 in real time, Col. 8, lines 3-6; *bridge/graphics controller 511 receives frame buffer access requests alternatively from one or more agents connected to the system bus 501 or from agents connected to the expansion bus 529*, Col. 8, lines 29-32; *byte reordering logic 657 is provided at the interface to the frame buffer 517, the byte reordering logic 657 writes and reads pixel data in a standard format (e.g., big-endian) regardless of the format in which an agent, such as the video input device 531, creates or expects to receive them (Figure 6A)*, Col. 10, line 61-Col. 11, line 1; *Figure 6A is a block diagram of the overall data flow within the bridge/graphics controller*, Col. 6, lines 61-64; Col. 20, lines 41-47; *frame buffer 517 has a SAM for supplying a serial stream of pixel data, the SAM ports 521 are configured to provide a datapath to a RAMDAC 523, which read the serial stream of pixel data from the SAM 521*, Col. 7, lines 49-58).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson so that the step of enabling the secondary processor to access the data comprises the steps of predefining a secondary storage space that is accessible to the secondary processor; causing the primary processor to store the data in the first predefined order in a primary storage space that is accessible to both the primary processor and the secondary processor; and causing the secondary processor to copy the data in the first predefined order from the primary storage space to the secondary storage space as suggested by Childers because Childers suggests the advantage of being able to write intelligible pixels into a frame buffer from a source on either of two endian-incompatible buses (Col. 5, lines 37-39).

13. With regard to Claim 7, Wilson does not teach that the step of determining the subdivisions comprises the steps of determining a size of each subdivision as a function of the predefined size of each datum of the data; and determining a number of subdivisions within the data. However, Childers discloses that the step of determining the subdivisions comprises the steps of determining a size of each subdivision as a function of the predefined size (2 bytes) of each datum (pixel) of the data (Col. 4, lines 61-64; Figures 4A, 4B; *64-bit wide bus*, Col. 8, lines 32-42); and determining a number of subdivisions (4) within the data (Col. 9, lines 31-38). This would be obvious for the same reasons given in the rejection for Claim 1.

14. With regard to Claim 12, Wilson does not specifically teach the step of displaying the data arranged in the second predefined order. However, Childers discloses the step of displaying the data arranged in the second predefined order (Col. 8, lines 36-43).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson to include the step of displaying the data arranged in the second predefined order as suggested by Childers because Childers suggests that if the video input device is connected to a bus that is incompatible with the bus connected to the display, the data must be reordered in order to be displayed (Col. 3, lines 15-25).

15. With regard to Claim 13, Wilson discloses fetching commands using a DMA controller (Col. 4, lines 7-10), and therefore the commands are inherently fetched from a memory medium, and therefore there is a memory medium on which are stored machine instructions for carrying out the steps.

16. Claims 8-11 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilson (US005960213A) and Childers (US005793996A) in view of Baldwin (US005594854A).

17. With regard to Claim 8, Wilson and Childers are relied upon for the teachings as discussed above relative to Claim 1.

However, Wilson and Childers do not teach the step of determining coordinates of each subdivision comprises the step of determining vertices of each subdivision relative to an origin of the data. However, Baldwin discloses reordering data from big-endian order to little-endian order (Col. 23, lines 20-29) and preserving the order of the pixels as well as the byte ordering within each pixel (Col. 23, lines 42-49). The data is subdivided into blocks or triangles (Col. 38, lines 52-53; Col. 31, lines 14-15; Col. 35, lines 53-64). Baldwin discloses the step of determining coordinates of each subdivision comprises the step of determining vertices of each subdivision relative to an origin of the data (Col. 32, lines 41-49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Wilson and Childers to include the step of determining coordinates of each subdivision comprises the step of determining vertices of each subdivision relative to an origin of the data as suggested by Baldwin because Baldwin suggests the advantage of being able to perform simple add operations so that no new arithmetic elements are needed (Col. 5, lines 26-61).

18. With regard to Claim 9, Wilson does not teach that the step of causing the secondary processor to perform the operation comprises the step of instructing the secondary processor to transpose the coordinates of each subdivision so as to mirror the data of each subdivision about a center position. However, Baldwin discloses that the step of causing the secondary processor to perform the operation comprises the step of instructing the secondary processor to transpose the coordinates of each subdivision so as to mirror the data of each subdivision about a center position (Col. 39, lines 35-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson so that the step of causing the secondary processor to perform the operation comprises the step of instructing the secondary processor to transpose the coordinates of each subdivision so as to mirror the data of each subdivision about a center position as suggested by Baldwin because Baldwin suggests the advantage of being able to reorder the data without complex processing (Col. 39, lines 35-45).

19. With regard to Claim 10, Wilson does not teach predefining a mask for selectively retaining a subset of the data; and applying the mask to the subdivisions to further subdivide the data into a plurality of subsets of data that are iteratively repositioned to new locations relative to the new positions, the new locations corresponding to original locations relative to the original positions. However, Baldwin discloses predefining a mask for selectively retaining a subset of the data; and applying the mask to the subdivisions to further subdivide the data into a plurality of subsets of data that are iteratively repositioned to new locations relative to the new positions,

the new locations corresponding to original locations relative to the original positions (Col. 51, lines 11-22).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson to include predefining a mask for selectively retaining a subset of the data; and applying the mask to the subdivisions to further subdivide the data into a plurality of subsets of data that are iteratively repositioned to new locations relative to the new positions, the new locations corresponding to original locations relative to the original positions as suggested by Baldwin because Baldwin suggests that this defines the limits of the block to be written, thereby reducing the amount of processing that must be performed (Col. 51, lines 11-22).

20. With regard to Claim 11, Wilson does not teach the step of determining a portion of data that changed since a previous execution cycle so that only the portion of data that changed since the previous execution cycle is reordered between the first predefined order and the second predefined order. However, Baldwin discloses that when a begin-draw command is sent, the internal registers are updated, but if a continue-draw command is sent, then this update does not happen and drawing continues with the current values in the internal registers (Col. 13, lines 27-31). Therefore, the reordering only occurs when the data is changed. Therefore, Baldwin inherently discloses the step of determining a portion of data that changed since a previous execution cycle so that only the portion of data that changed since the previous execution cycle is reordered between the first predefined order and the second predefined order (Col. 13, lines 27-31; Col. 23, lines 20-29, 37-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Wilson to include the step of determining a portion of data that changed since a previous execution cycle so that only the portion of data that changed since the previous execution cycle is reordered between the first predefined order and the second predefined order as suggested by Baldwin because Baldwin suggests the advantage of eliminating unnecessary processing (Col. 31, lines 27-31).

21. With regard to Claim 14, According to the disclosure of this application, reordering the data using an operation that was not provided for that purpose involves using texture operations to perform the reordering (page 11, lines 20-22). Wilson discloses that the GLINT Delta performs operations such as texture operations (Col. 2, lines 47-62), and the GLINT Delta reorders data between a first predefined order and a second predefined order (Col. 2, lines 43-64; Col. 4, lines 20-25; Col. 20, lines 4-10), and therefore this is done using an operation not provided to the system for that purpose. Wilson discloses a primary processor (host processor); a secondary processor (GLINT Delta) in communication with the primary processor (Col. 3, lines 60-62); and a memory in communication with the primary processor and the secondary processor, the memory storing the data in the first predefined order (Col. 3, line 60-Col. 4, line 25). Commands are fetched using a DMA controller (Col. 4, lines 7-10), and therefore the commands are inherently fetched from the memory, and therefore machine instructions are stored that cause the primary processor and the secondary processor to carry out a plurality of functions, including accessing the data that are arranged in the first predefined order with the secondary processor (Col. 2, lines 43-64; Col. 4, lines 20-25; Col. 20, lines 4-10).

However, Wilson does not teach determining subdivisions of the data that are arranged in the first predefined order, wherein each subdivision is based on a predefined size of each datum of the data; determining original positions of coordinates defining each subdivision within the data that are arranged in the first predefined order; and using the secondary processor for performing the operation, thereby transforming the coordinates of each subdivision to new positions and repositioning the data of each subdivision to have the same locations relative to the new positions as the data had relative to the original positions, thereby reordering the data from the first predefined order to the second predefined order. However, Childers discloses that each pixel contains 2 bytes (16 bits) of data (Col. 4, lines 61-64; Figures 4A, 4B). The data are subdivided into half-words (16 bits) in order to ensure that pixels are presented in a uniform format regardless of the endian characteristic of the bus from which they were received or of the software or apparatus that generated the pixels (Col. 8, lines 32-42), so that the pixels themselves do not become "scrambled" as a result of their bytes being swapped (Col. 4, line 48-Col. 5, line 16). Therefore, Childers discloses determining subdivisions of the data that are arranged in the first predefined order (little-endian, Col. 20, lines 40-45; Col. 8, lines 36-42), wherein each subdivision is based on a predefined size (2 bytes) of each datum (pixel) of the data (Col. 4, lines 61-64; Col. 8, lines 32-42); determining original positions of coordinates defining each subdivision within the data that are arranged in the first predefined order; and using the secondary processor for performing the operation, thereby transforming the coordinates of each subdivision to new positions and repositioning the data of each subdivision to have the same locations relative to the new positions as the data had relative to the original positions, thereby reordering the data from the first predefined order to the second predefined order (Col. 17, line

54-Col. 18, line 2). This would be obvious for the same reasons given in the rejection for Claim 1.

However, Wilson and Childers do not teach that the primary processor determines subdivisions of the data; using the primary processor, determining original positions of the subdivisions within the data. However, Baldwin discloses that the framebuffer bypass determines subdivisions of the data; using the framebuffer bypass, determining original positions of the subdivisions within the data (Col. 23, lines 20-29, 37-51). The host processor controls the framebuffer bypass to access the frame buffer (Col. 21, lines 28-46), and therefore the primary processor is doing this.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Wilson and Childers so that the primary processor determines subdivisions of the data; using the primary processor, determining original positions of the subdivisions within the data as suggested by Baldwin because Baldwin suggests the advantage of having the primary processor directly access the frame buffer for faster processing (Col. 21, lines 28-46).

22. With regard to Claim 15, Claim 15 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

23. With regard to Claim 16, Wilson does not teach that the machine instructions further cause the processor to perform the functions of determining a size of each subdivision as a function of the predefined size of each datum of the data; and determining a number of

subdivisions within the data. However, Childers discloses that the machine instructions further cause the processor to perform the functions of determining a size of each subdivision as a function of the predefined size (2 bytes) of each datum (pixel) of the data (Col. 4, lines 61-64; Figures 4A, 4B; Col. 8, lines 32-42); and determining a number of subdivisions (4) within the data (Col. 9, lines 31-38). This would be obvious for the same reasons given in the rejection for Claim 1.

However, Wilson and Childers do not teach that the primary processor determines the subdivision. However, Baldwin discloses that the primary processor determines the subdivisions (Col. 23, lines 36-51; Col. 21, lines 28-46). This would be obvious for the same reasons given in the rejection for Claim 14.

24. With regard to Claim 17, Wilson does not teach that the machine instructions further cause the primary processor to perform the function of determining vertices of each subdivision relative to an origin of the data. However, Baldwin discloses reordering data from big-endian order to little-endian order (Col. 23, lines 20-29) and preserving the order of the pixels as well as the byte ordering within each pixel (Col. 23, lines 42-49). The data is subdivided into blocks or triangles (Col. 38, lines 52-53; Col. 31, lines 14-15; Col. 35, lines 53-64). Baldwin discloses that the machine instructions further cause the primary processor to perform the function of determining vertices of each subdivision relative to an origin of the data (Col. 13, lines 16-17, 53-55). This would be obvious for the same reasons given in the rejection for Claim 8.

25. With regard to Claim 18, Claim 18 is similar in scope to Claim 9, and therefore is rejected under the same rationale.

26. With regard to Claim 19, Wilson does not teach that the machine instructions further cause the primary processor to perform the function of predefining a mask for selectively retaining a subset of the data and cause the secondary processor to perform the function of applying the mask to the subdivisions to further subdivide the data into a plurality of subsets of data that are iteratively repositioned to new locations relative to the new positions, the new locations corresponding to original locations relative to the original positions. However, Baldwin discloses that the machine instructions further cause the primary processor to perform the function of predefining a mask for selectively retaining a subset of the data and cause the secondary processor to perform the function of applying the mask to the subdivisions to further subdivide the data into a plurality of subsets of data that are iteratively repositioned to new locations relative to the new positions, the new locations corresponding to original locations relative to the original positions (*graphics system can do masked block writes of variable length (e.g. 8, 16, or 32 pixels), hardware masking logic, thus the rasterizer can step by the Block Fill increment*, Col. 51, lines 11-22; *hardware write masks are controlled using the FBHardwareWriteMask register*, Col. 53, lines 39-40; *control registers are updated only by the host*, Col. 13, lines 16-17). This would be obvious for the same reasons given in the rejection for Claim 10.

27. With regard to Claim 20, Wilson does not specifically teach a display in communication with the secondary processor, wherein the machine instructions further cause the secondary processor to perform the function of displaying the data arranged in the second predefined order on the display. However, Childers discloses a display (515, Figure 5) in communication with the secondary processor (511), wherein the machine instructions further cause the secondary processor to perform the function of displaying the data arranged in the second predefined order on the display (Col. 8, lines 36-43). This would be obvious for the same reasons given in the rejection for Claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER